WHAT IS CLAIMED IS:

1. A synchronized sampled data system, comprising:

a shared data bus providing an instructional word; and

a first sampled data circuit and a second sampled data circuit each receiving the instructional word on the shared data bus, each said first circuit and said second circuit having an output phase shifted from the other as a function of at least one control signal provided to each said circuit via said shared data bus.

2. The system as specified in claim 1 wherein each said first circuit and said second circuit have a respective counter, each said counter having a different count as a function of a common said control signal.

3. The system as specified in claim 1 wherein a different predetermined start count is preloaded into each of the first circuit and the second circuit upon an in initialization of the sampled data system.

4. The system as specified in claim 2 wherein each of the first circuit and second circuit are clocked by a common clock signal to produce the phase shifted outputs, the phase shift of the outputs being correlated to the difference in counts between the respective counter.

5. The system as specified in claim 1 wherein the outputs of the first and second circuits are shifted 180° from each other.

6. The system as specified in claim 4 wherein the circuit outputs continuously maintain the phase shift when a continuously clocked by the clock signal.

7. The system as specified in claim 1 wherein each said first and second circuit comprise a power converter.

8. The system as specified in claim 7 wherein the outputs of the first and second circuits are shifted 180° from each other.

9. The system as specified in claim 8 wherein noise generated by each said power converter is staggered.

10. The system as specified in claim 9 wherein noise generated at switching instants of each said power converter occurs at twice the repetition rate and less current as compared to unstaggered synchronized power converters.

11. The system as specified in claim 7 wherein each said power converter has multiple outputs each being phase shifted with respect to the outputs of the other power converter.

12. The system as specified in claim 7 wherein each said power converter includes an integrator circuit having a value corresponding to a phase of the respective circuit.

13. The system as specified in claim 1 wherein each said first and second circuit have a plurality N of common control signals.

14. The system as specified in claim 13 wherein a selection of available shifts of the first and second circuit is 2^N.

15. The system as specified in claim 13 further comprising a total of 2^N sampled data circuits, where N is 2 or greater.

16. The system as specified in claim 4 wherein the phase shift between the first and second circuit has a granularity of 1/M clock cycles, where M is the number of clock cycles in a count interval.

17. The system as specified in claim 1 wherein each said first and second circuit comprises an A to D converter.

18. A method of phase shifting two or more sampled data circuits sharing a common databus, comprising the steps of:

operating a first and second sampled data circuit to have a phase shift from one another being a function of at least one control signal provided to each via the common databus.

19. The method as described in claim 18 further comprising the step of loading a different count into a counter of each said first and a second sampled data via the common databus.

20. The method as described in claim 19 wherein the control signal is provided on at least one common signal line to each of the first and second circuits.

21. The method as described in claim 20 futher comprising N common signal lines, wherein a selection of available phase shifts between the first and second circuit is 2^N.

22. The method as described in claim 19 wherein each of the first and second circuits have a counter clocked by a common clock signal, wherein the phase shift between the first and second circuit has a granularity of 1/M clock cycles, where M is the number of clock cycles in a count interval.

23. The method as described in claim 18 wherein a different predetermined start count is preloaded into a counter of each of the first circuit and the second circuit upon initialization of the sampled data system.

24. The method as described in claim 19 wherein the counters of each of the first and second data circuits are clocked by a common clock signal to produce the phase shifted outputs, the phase shift of the outputs being correlated to the difference in counts of the respective counter.

25. The method as described in claim 18 further comprising a total of 2^N sampled data circuits, where N is 2 or greater.

26. The method as described in claim 25 wherein the outputs of each said sampled data circuit continuously maintain a predetermed phase shift upon a continuous clock of a clock signal.

27. The method as described in claim 18 wherein each said first and second circuit comprise a power converter.

28. The method as described in claim 27 wherein the outputs of the first and second circuits are shifted 180° from each other.

29. The method as described in claim 27 wherein noise generated by each power converter is staggered.

30. The method as described in claim 29 wherein noise generated by thepower converters at switching instants occurs at twice the repetition rate and half the current as compared to unstaggered synchronized power converters.

31. The method as described in claim 27 wherein each said power converter has multiple outputs each being phase shifted with respect to the outputs of the other power converter.

32. The method as described in claim 27 wherein each said power converter includes a ramp circuit having a value corresponding to a phase of the respective circuit.

33. The method as described in claim 18 wherein each first and second circuit have a plurality N of common control signals.

34. The method as specified in claim 18 wherein each said first and second circuit comprises an A to D converter.